FIGS. **4A–4F** are schematic cross-sectional diagrams illustrating the steps of another process for producing a TFT-LCD panel according to the present invention. A buffer layer **4021** and a light-shielding layer are formed on a light-transmissible substrate **400** in sequence. Subsequently, a masking and photolithographic process proceeds to define a light-shielding structure **401**, as shown in FIG. **4A**. Please refer to FIG. **4B**. Another buffer layer **4022** and an amorphous silicon (a-Si:H) layer are successively formed on the buffer layer **4021** with the light-shielding structure **401**. Then, the amorphous silicon layer is converted into a polysilicon layer **404** by a laser crystallizing process. It is understood that the material for forming the buffer layers **4021** and **4022** may be the same or different. The following steps for producing the top-gate TFT structure and the function of the light-shielding structure as shown in FIGS. **4C–4F** are similar to those shown in FIGS. **3D–3G**, so it would not be describe again herein. The numeral references **405**, **406**, **407**, **408**, **409**, **410**, **411**, **412** labeled in FIGS. **4C–4F** indicate a photoresist mask structure, source/drain regions, a gate insulating layer, a gate conductive structure, LDD regions, a dielectric layer, a source/drain connecting line structure and a channel region, respectively.

In above embodiments, the light-transmissible substrate can be a light-transmissible glass. The conductive layer is formed of chromium (Cr), tungsten molybdenum (WMo), tantalum (Ta), aluminum (Al) or copper (Cu) by a sputtering procedure, and typically has thickness of around 200 nm. The buffer layer is formed of silicon nitride, silicon oxide or the combination thereof by plasma enhanced chemical vapor deposition (PECVD) and typically has thickness of around 600 nm. The light-shielding layer is formed of an opaque material having a relatively high melting point, e.g. chromium (Cr), molybdenum (Mo), or tungsten (W), by a sputtering procedure, and preferably has thickness of around 600 nm. The light-shielding layer can also be formed of organic material. The amorphous silicon layer is generally annealed and dehydrogenated for 30 minutes in a high temperature furnace before the laser crystallizing process, which performs 100 shots with the energy of 400 mJ/cm^2. The thickness of the amorphous silicon layer is typically around 50 nm. The heavily doping ion implantation procedure is performed with As or P ions as dopants under a dosage of around 1×10^{15} cm^{-2}. The trace N-type dopant implantation procedure is performed under a dosage of around 1×10^{13} cm^{-2}. The gate insulating layer is formed by plasma enhanced chemical vapor deposition (PECVD) and, generally, formed of silicon oxide, and typically has a thickness of around 100 nm.

In addition, the light-shielding structure according to the present invention is used not only for shielding the illumination of the back light source but also as a black matrix. Thus, no extra producing and aligning steps are required to provide a black matrix.

To sum up, the present invention provides a light-shielding structure, which is disposed upstream of the buffer layer in the light direction or incorporated into the buffer layer structure, to block the illumination of the back light source from adversely affecting the channel region. Therefore, the generation of the photoelectric current in the channel region can be efficiently controlled, and the current leakage problem can be avoided. In addition, since the back exposure technique is applied, a low temperature polycrystalline silicon (LTPS) TFT structure can be produced without increasing the masking numbers.

While the invention has been described in terms of what is presently considered to be the most practical and preferred embodiments, it is to be understood that the invention needs not be limited to the disclosed embodiment. On the contrary, it is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims which are to be accorded with the broadest interpretation so as to encompass all such modifications and similar structures.

What is claimed is:

1. A structure of a thin film transistor (TFT) planar display panel comprising:

a light-transmissible substrate;

a buffer layer formed on said light-transmissible substrate;

a top-gate TFT structure formed on said buffer layer and including a channel region; and

a light-shielding structure formed between a back light source of said thin film transistor planar display panel and said top-gate TFT structure and electrically isolated from said top-gate TFT structure, and an area of said light-shielding structure being substantially aligned with and generally coextensive with said channel region for protecting said channel region from illumination of said back light source.

2. The structure according to claim **1** wherein said light-transmissible substrate is a glass substrate.

3. The structure according to claim **1** wherein said buffer layer is formed of a material selected from a group consisting of silicon nitride, silicon oxide, and a combination thereof.

4. The structure according to claim **1** wherein said light-shielding structure is formed between said back light source and said buffer layer.

5. The structure according to claim **1** wherein said light-shielding structure is formed in said buffer layer.

6. The structure according to claim **1** further comprises a black matrix which is implemented by said light-shielding structure.

7. The structure according to claim **1** wherein said top-gate TFT structure is a low temperature polycrystalline silicon (LTPS) TFT structure.

8. The structure according to claim **1** wherein said light-shielding structure is formed of an opaque material having a relatively high melting point.

9. The structure according to claim **8** wherein said light-shielding structure is formed of a material selected from a group consisting of chromium (Cr), molybdenum (Mo), tungsten (W) and organic material.

10. The structure according to claim **1** wherein said top-gate TFT structure includes:

a semiconductor layer formed on said buffer layer and formed therein said channel region and source/drain regions;

a gate insulating structure formed on said semiconductor layer;

a gate conductive structure formed on said gate insulating structure above said channel region;

a dielectric layer formed on said gate conductive structure and said gate insulating structure; and

a conductive line structure formed on said dielectric layer and penetrating through said gate insulating structure and said dielectric layer to contact with said source/drain regions in said semiconductor layer.

11. The structure according to claim **10** further comprising lightly doped drain regions disposed next to said source/drain regions and sandwiching therebetween said channel region.

12. The structure according to claim **10** wherein said semiconductor layer is a polycrystalline silicon layer.